REMARKS

Claims 76, 84 and 96 are amended. New claims 102-108 are added. Claims 76-108 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

Claim 84 stands rejected under 35 U.S.C. §112, second paragraph, for lacking antecedent basis to "one region." The Examiner is mistaken. Claim 84 depends from claim 82 which depends from independent claim 76. Independent claim 76 recites one of a source region or a drain region elevationally above the channel region, the one region comprising.... Consequently, antecedent basis is provided in claim 76, and therefore, the rejection is inappropriate and must be withdrawn.

Claim 93 stands rejected under 35 U.S.C. §112, second paragraph, for lacking antecedent basis to "the first thin film S/D region and the second thin film S/D region." The Examiner is mistaken. Claim 93 depends from claim 92 which depends from independent claim 86. Independent claim 86 recites a first thin film source/drain (S/D) region and a second thin film S/D region. Consequently, antecedent basis is provided in claim 86, and therefore, the rejection is inappropriate and must be withdrawn.

Claims 76-101 stand rejected under 35 U.S.C. §102(b) as being anticipated by Banerjee (4,864,374).

Regarding independent claim 76, such claim recites a gate in lateral proximity to a channel region, the gate comprising an annulus which laterally ncircl s the laterally proximate channel region. Banerjee teaches a two-

transistor cell 8 that includes a pass transistor 12 driven by a word line 16 and a gain transistor 24 (col. 4, lns. 1-40) having a gate 18 (also the storage node of a capacitor) (col. 5, lns. 64-66). Word line 16 is the gate for pass transistor 12 (col. 6, lns. 1-4). However, no gate of Banerjee **comprises an annulus** as positively stated in claim 76. Gate 16 of the pass transistor is of a solid construction and gate 18 of the gain transistor 24 is of a solid construction (Figs. 2, 3-7). Consequently, it is inconceivable that the gate constructions of Banerjee could be reasonably or fairly stated to teach or suggest a gate comprising an annulus as positively recited in claim 76. Banerjee fails to teach or suggest a positively recited limitation of claim 76. For at least this reason, claim 76 is allowable.

Moreover, Banerjee fails to teach or suggest a **gate** comprising an annulus which laterally **encircles** the laterally proximate channel region. Gate 84 of Banerjee is a solid construction and does not encircle any structure (Fig. 13; col. 10, lns. 20-68 to col. 11, lns. 1-20). Gate 18 of Banerjee is a solid construction extending through a channel layer 34 and does not encircle any structure (Fig. 13; col. 9, lns. 25-35 (referring to Fig. 3 and col. 5, lns. 56-60)). Accordingly, it is inconceivable that Banerjee teaches or suggests a **gate** which **encircles** the channel region as positively recited in claim 76. Banerjee fails to teach or suggest another positively recited limitation, and therefore, claim 76 is allowable.

Claims 77-85 and 102-103 depend from independent claim 76, and therefore, are allowable for the reasons discussed above with respect to the

independent claim, as well as for their own recit d features which are not shown or taught by the art of record.

For example, claim 81 recites a channel region comprising an annulus encircled by a gate. Banerjee teaches just the opposite, that is, a channel surrounding a solid gate construction (col. 7, lns. 65-68 to col. 8, lns. 1-15), which does not teach or suggest a channel region **encircled by** a gate as positively recited in claim 81. Since Banerjee fails to teach or suggest a positively recited limitation of claim 81, such claim is allowable.

Further, dependent claim 82 recites an **opening extending through** the a gate electrode layer. Each embodiment of Banerjee teaches forming a trench (30, 68 respectively) formed through layers, and then filling each trench with two sets of **solid gate material** (gates 16, 18 and 84). Accordingly, it is inconceivable that Banerjee teaches or suggests an **opening extending through** a gate electrode layer as positively recited in claim 82. For at least this reason, claim 82 is allowable.

Regarding independent claim 86, such claim recites a gate comprising an annulus which laterally encircles a laterally proximate thin film channel region. Banerjee fails to teach or suggest a gate comprising an **annulus.** For at least reason, claim 86 is allowable. Furthermore, Banerjee fails to teach or suggest a gate **encircles** a laterally proximate **thin film channel region** as positively recited in claim 86. For this additional reason, claim 86 is allowable.

Claims 87-95 and 104-105 depend from independent claim 86, and therefore, are allowable for the reasons discussed above with respect to the

independent claim, as well as for their own recited f atures which are not shown or taught by the art of record.

Regarding independent claim 96, Banerjee fails to teach or suggest the recited combination of limitations of claim 96. First, respectfully, the mis-characterization of the Banerjee teachings must be addressed. The Examiner relies on layer 26 of Banerjee to teach a gate electrode layer recited in claim 96 (pg. 3 of paper no. 20). However, regarding layer 26, Banerjee teaches a "heavily doped N+ read bit line 26 and the heavily doped N+ substrate 20 form the respective source and drain regions of the gain transistor 24" (col. 5, lns. 60-65). That is, layer 26 of Banerjee is a **source region** for transistor 24, not a gate electrode as stated by the Examiner. In no fair or reasonable interpretation does the disclosed construction of layer 26, which is clearly taught as a source region, teach or suggest a gate electrode.

Consequently, Banerjee fails to teach or suggest an opening defining **opposing sidewalls in a gate electrode layer** as positively recited in claim 96. Banerjee teaches forming trenches (30, 68) and then forming gate dielectrics (32, 70) along the sidewalls of the trenches. Next, Banerjee teaches providing solid gate material 18 in the trenches adjacent the gate dielectrics (Figs. 7 and 13). Consequently, the gate dielectrics (32, 70) define the sidewalls of the Banerjee gates, not an opening. In no fair or reasonable interpretation does Banerjee teach or suggest an **opening** defines the opposing sidewalls in a **gate electrode layer** as positively recited in claim 96. For at least this reason, claim 96 is allowable.

Moreover, Banerjee fails to teach or sugg st, a gate dielectric layer disposed over a portion of the sidewalls as an annulus, **and** a channel region disposed within the opening as positively recited in claim 96. Only the gain transistor (Figs. 7 and 13) has a gate dielectric layer (32, 70 respectively) over sidewalls of a trench (30, 68 respectively). However, the gain transistor has layer 34 as a channel region which is located **outside** the trench (col. 5, lns. 55-69; Figs. 7 and 13), and therefore, fails to teach or suggest a channel region disposed **within** the opening as positively recited in clam 96. To the contrary, Banerjee teaches gate 18 is disposed within the trench, not the channel region. Since Banerjee fails to teach or suggest a positively recited limitation of claim 96, claim 96 is allowable.

Additionally, claim 96 recites a gate electrode layer comprises an opening. Banerjee teaches forming trenches and filling the trenches with solid gate material. Accordingly, it is inconceivable that Banerjee teaches or suggests a gate electrode layer comprises an **opening** as positively recited in claim 96. Claim 96 is allowable for this additional reason.

Claims 97-101 and 106-108 depend from independent claim 96, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

For example, claim 99 recites a channel region **essentially fills** the **opening**. Banerjee teaches a transistor 12 has a channel formed by a P^- portion of layer 56 that minutely fills trench 30 (col. 7, lns. 65-68 to col. 8, lns.

1-15; Figs. 6-7). Banerj e also teaches a transistor 76 has a chann l 82 that minutely fills trench 68 (Fig. 13; col. 10, lns. 25-55). In no fair or reasonable interpretation does Banerjee teach or suggest a channel region **essentially fills** the **opening** as positively recited in claim 99. Claim 99 is allowable.

Moreover, claim 100 recites a channel region essentially fills the opening. Banerjee fails to teach or suggest the is positively recited limitation, and therefore, claim 100 is allowable.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

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D. Brent Kenady
Reg. No. 40,045